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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,427	07/13/2004	Johannes Hubertus Antonius Brekelmans	NL 020021	9429

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/501,427	BREKELMANS ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☒ Claim(s) 1 and 3-6 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 7/13/2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/13/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*Dr*awings

The drawings are objected to under 37 CFR 1.83(a). Fig. 2 is misdescriptive, it only shows one half of the claimed differential inverter. Fig. 2 only has one transistor pair, and would not be able to supply the differential outputs as recited in claim 1. It is suggested that the missing second pair be shown in Fig.2, or that Fig. 2 be deleted.

It should also be noted that a dot representing a connection to the line labeled OUT 2 and the drains of M'1 and M'2 must be shown. Additionally, Fig. 7 requires a label that reads -- PRIOR ART --.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim objections

Claim 1 is objected to because of the following informalities: The recitation of "indicative for" of line 19 is confusing. It is suggested that it be changed to -- indicative of --. Appropriate correction is required.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the second vector" in line 10. There is no antecedent basis for this limitation in the claim. It is suggested that "the second vector" be changed to -- the second pair --. Claims 2-6 are rejected based on their dependency to claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Weekes et al. (USPN 3,582,802).

With respect to claim 1, Weekes et al. (USPN 3,582,802) discloses in Fig. 2, a differential inverter comprising a differential inverter (49, and input transistors 44, 46)

- a differential input for receiving a first pair of signals comprising a first input signal (signal input to the control gate of 44) and a second input signal (signal input to the control gate of 46)

- a differential control input for receiving a second pair of input signals comprising a first control signal (the emitter of 44 receives a bias signal from 48 through resistor 38) and a second control signal (the emitter of 46 receives a bias signal from 48 through resistor 40),

- a differential output for transmitting a third vector of differential signals comprising a first output signal (signal at node 16) and a second output signal (signal at node 18)

- said differential inverter being characterized in that it further comprises a controlled bias generator (48 is controlled by the voltage divided signal) generating the second vector of input signals in response to a bias control signal (it can be seen that 48 generates the bias signals of 44 and 46, at the node between resistors 38 and 40) which is generated at an output of a voltage divider coupled to the differential output of

the differential inverter (Resistors 28 and 30 create a voltage divider, which creates a bias signal at node 26 that is input to 48. It can be seen that the bias signal is created from the first and second output voltages, because the voltage divider is connected to nodes 16 and 18.) said bias control signal being indicative of a DC voltage of the of the differential output (A DC signal will be present between at node 16 and 18. This DC voltage will be input to 48 at node 26. Thus, the bias control will be indicative of a DC voltage.).

With respect to claim 2, it can be seen that resistors 28 and 30 are connected together at node 26, and that 28 is connected to the first output and 18 is connected to the second output. Also, node 26 outputs a bias signal to bias generator 48. Weekes et al. discloses that the resistance of 28 and 30 is Ra and Rb respectively. Thus, Weekes et al. discloses that the resistance of 28 and 30 can be any reasonable value, which includes values that are equal.

Allowable Subject Matter

Claims 3-6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to claim 3, there was no prior art found that disclosed a differential inverter that has a bias control signal input to a PMOS transistor through a resistive means, and second bias signal input to a NMOS transistor through another resistive means. Yin (USPN 5,705,946) disclosed a level-shifting device in Fig. 4 that has two

differential inverters that receive input and bias signals. However, there is no motivation to use a level-shifting device for differential inverter 49. There was no cited prior art that taught motivation for replacing Weekes et al.'s generic differential inverter 49, with Yin's level shifter. There was also no other prior art found that disclosed the recited language of claim 3, and provided motivation to use it in a circuit that taught the recited language of claim 1. Thus claim 3 is allowable.

With respect to claim 4, There was prior art found that taught the using inverters to split a single input signal into two. However, there was no motivation provided by Weekes et al. to use the signal splitter in its bias circuit. For example Fig. 6 of Yamamoto et al. taught the using a inverter 38b to split a signal to two other inverters (40a and 40b), which are then input to a p and n type transistors 42 and 44. However, there is no motivation to use this type of buffer in place of that of buffer 48 in Weekes et al.. This is because 48 outputs a single signal which is split between two resistors, whereas Yamamoto et al. outputs two signals that are already split. There would be no motivation for adding more circuit components to Weekes et al., because it would be more expensive to manufacture and it would perform the same as the single buffer 48. Chiu et al (USPN 6,734,700) discloses the same situation as Yamamoto et al. in Fig. 1A, and it too doesn't supply any motivation to replace 48 of Weekes et al. with it. Additionally, Tang et al. (USPN 6,794,900) discloses a circuit that has two separate signals that are inverted being supplied to a differential input from the output through a two bias generators. However, these signals are not derived from a single bias signal, which is voltage divided at the between the outputs. Rather, they are derived straight

from each differential output. There is no motivation to voltage divide these signals to be input to a bias control. Therefore there would be no single bias signal to be sent to the signals splitters of Chiu et al. and Yamamoto et al. Thus, claim 4 is allowable, and claim 5 is allowable based on it dependency to claim 4.

With respect to claim 6, there was no prior art found that taught a differential amplifier with an "LC tank" coupled to its outputs and then feedback to the inputs of the differential inverter. There was prior art found that did have a differential inverter with an LC tank between its outputs, such as Fig. 1 of Smith et al. (USPN 6,043,710), Fig. 6 of Horiguchi et al (USPN 5,952,856), and Fig. 9 of Sugawara (USPN 5,495,194). Also, there was no prior art found that provided motivation for combining claim the teachings of Weekes et al. with the any of the cited prior art with LC tanks. No cited prior taught the further recitation a differential inverter having its outputs connected to a LC and cross-coupled to the input of the inverter. Thus, claim 6 is allowable.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Whitlock (USPN 5,568,561), in Fig. 12, and Yamauchi (USPN6,356,141), in Fig. 1, both have discloses that read over claims 1-2. It should also be noted that Fig 7(a) and (b) of Yamamoto et al. (UPSPN 5,672,983) disclose CMOS inverters with different PMOS and NOMS geometries.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)

272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TH
September 28, 2005